

TinyANC
Big quiet. Tiny chip.

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Custom ASIC for Adaptive Noise Cancellation

Eric Chang | Alex Huang | Spark Li | Roland Yin | Frank Yu

Background

TinyANC is a custom ASIC that brings adaptive noise cancellation to over-ear headphones. Two microphones capture ambient sound in real time, and the chip generates an opposing anti-noise signal that cancels external noise through destructive interference. Because effective cancellation demands sub-millisecond latency, it uses a time-domain FIR filter, continuously tuned by an LMS (Least Mean Squares) algorithm to adapt across a wide range of acoustic environments.

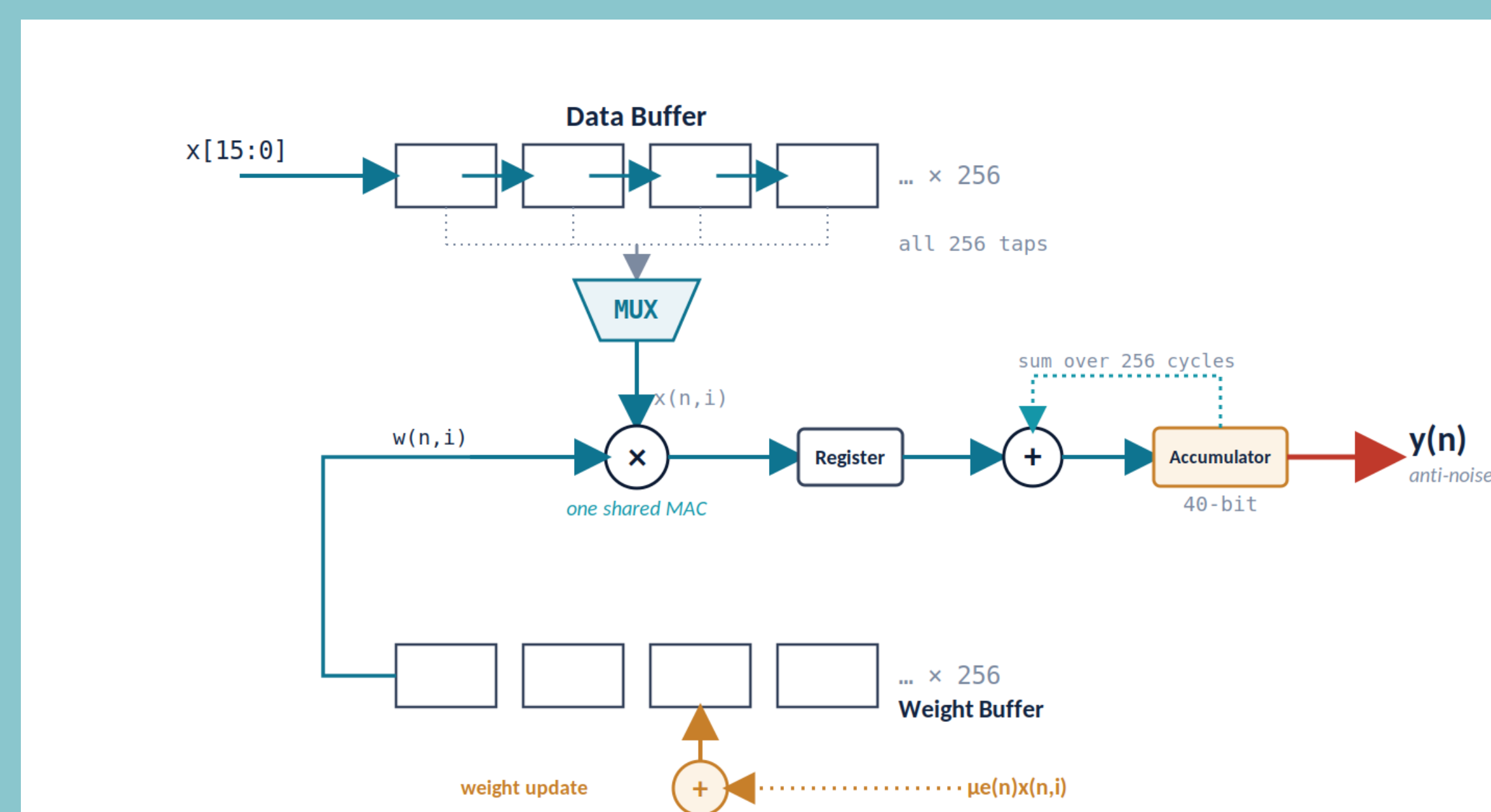


System architecture: passive cup path, adaptive FIR, and the LMS update loop

Signal Processing Steps

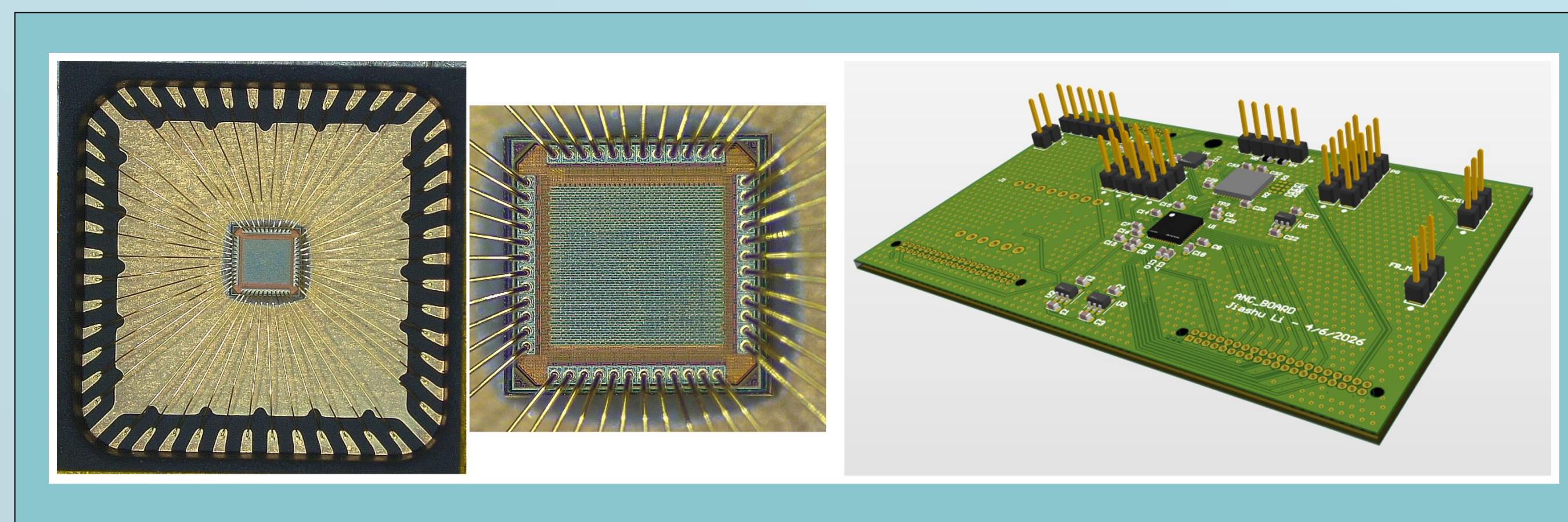
- **Detection:** an external mic monitors environmental noise while an internal mic measures the sound still reaching the ear.
- **Filtering:** a 256-tap FIR filter processes each incoming sample, producing a canceling signal in real time.
- **Actuation:** the LMS algorithm continuously fine-tunes the filter and drives the speaker to cancel any remaining noise.

FIR Filter Block Diagram



Pipelined datapath: one shared MAC reused across all 256 taps, summed in a 40-bit accumulator

Final Design — TinyANC

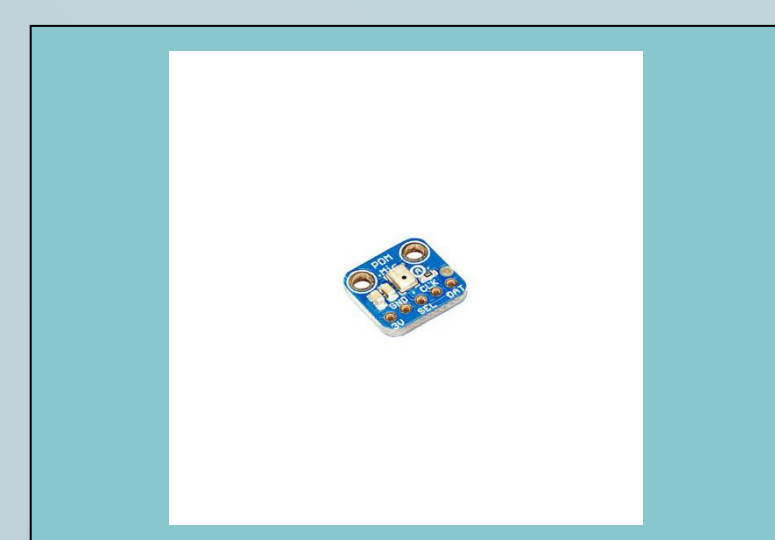


Fabricated 1 mm² ASIC, two views (left) and custom carrier PCB (right)

Key Features & Specs

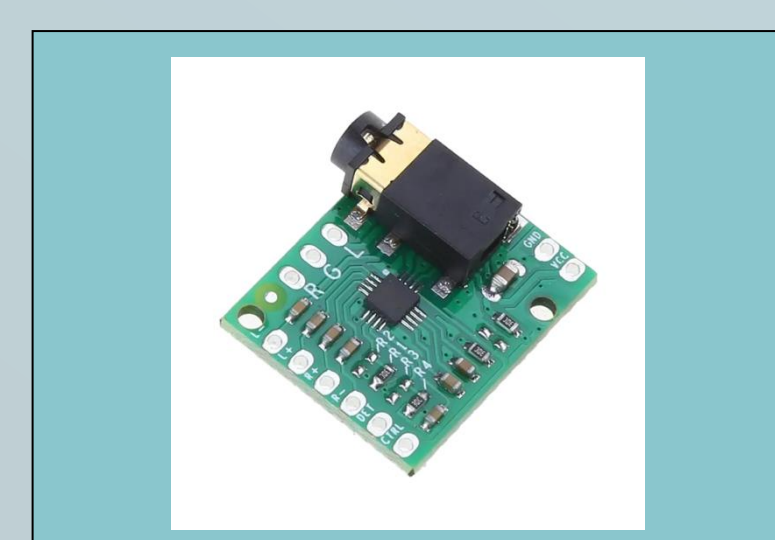
- 256-tap adaptive FIR + LMS, written in Verilog and verified in MATLAB/Simulink
- Pipelined datapath shares one MAC unit to fit the die area
- TSMC 65 nm, 1 mm² die (~360k gates), 48-lead QFN package
- On-chip scan + weight-bypass logic enables post-fabrication tuning

Hardware / Key Components



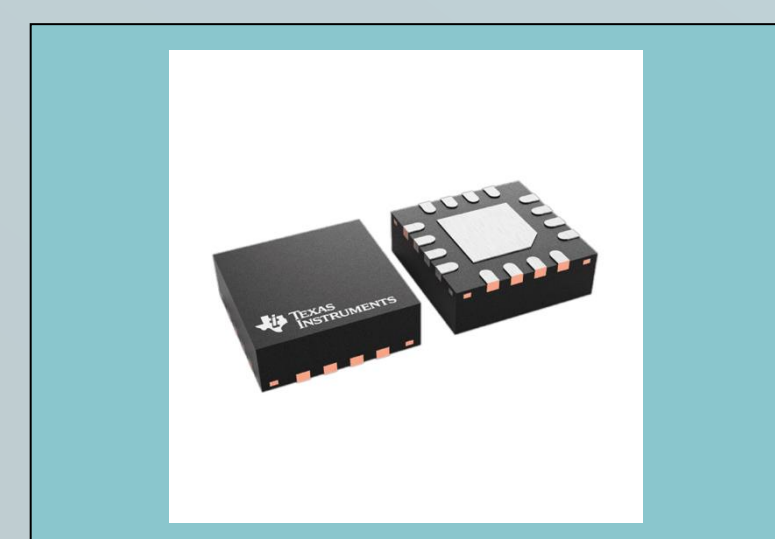
ST MP34DT01-M

PDM digital output, 61 dBA SNR, 60 Hz–15 kHz. Provides the reference and error mic inputs.



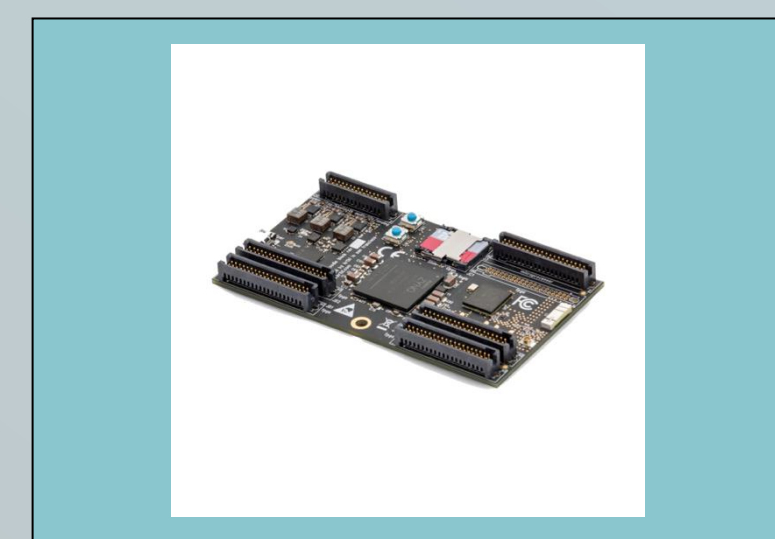
Adafruit PCM5102

Stereo 24-bit DAC, 8–384 kHz, 112 dB SNR. Converts the chip output back to analog.



TI TPA6132

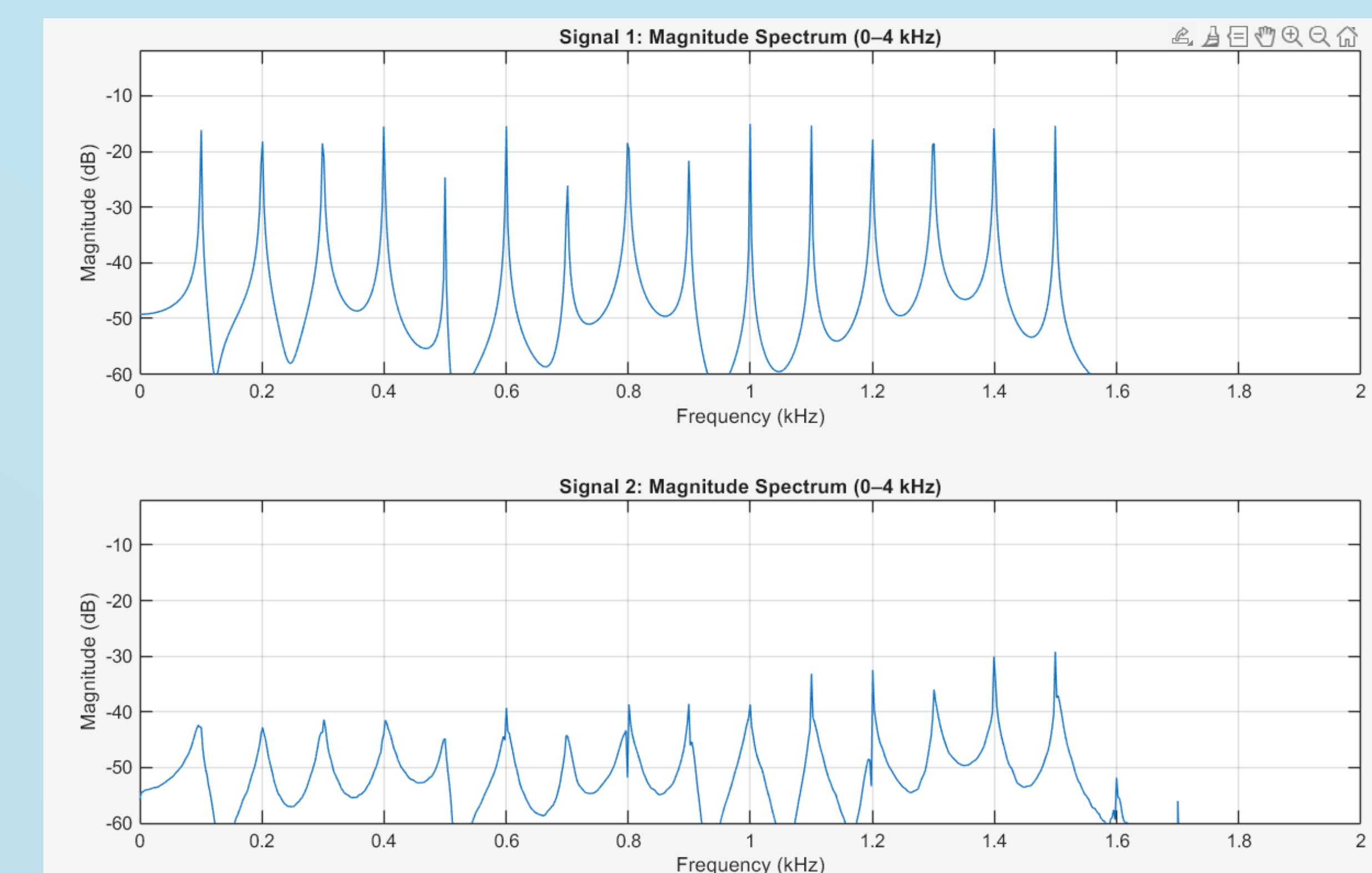
25 mW into 16 Ω load, 100 dB SNR, DirectPath ground-referenced output. Drives the headphones.



Xilinx Zynq (Snickerdoodle)

Runs the corrected LMS weight update off-chip and drives scan + bypass during bring-up.

Key Result — Noise Cancellation



Verified against an FPGA reference model. Above: FFT of pink noise (top) versus the residual after cancellation (bottom) — every tonal peak is pushed down, confirming **broadband attenuation across the target band**.

Results & Conclusions

- **Designed and fabricated** a headphone-grade ANC system on a custom ASIC implementing a 256-tap FIR filter.
- Measured **~10–20 dB attenuation below 200 Hz** and **~5–10 dB** across 200–1000 Hz on the FPGA reference.
- A post-tape-out rounding bug caused weight drift; a leaky-LMS update on the companion FPGA (via the built-in bypass path) **fixed it without re-spinning silicon**.
- Built-in scan and weight-bypass logic give **real-time visibility** into the chip's internal behavior for bring-up and tuning.

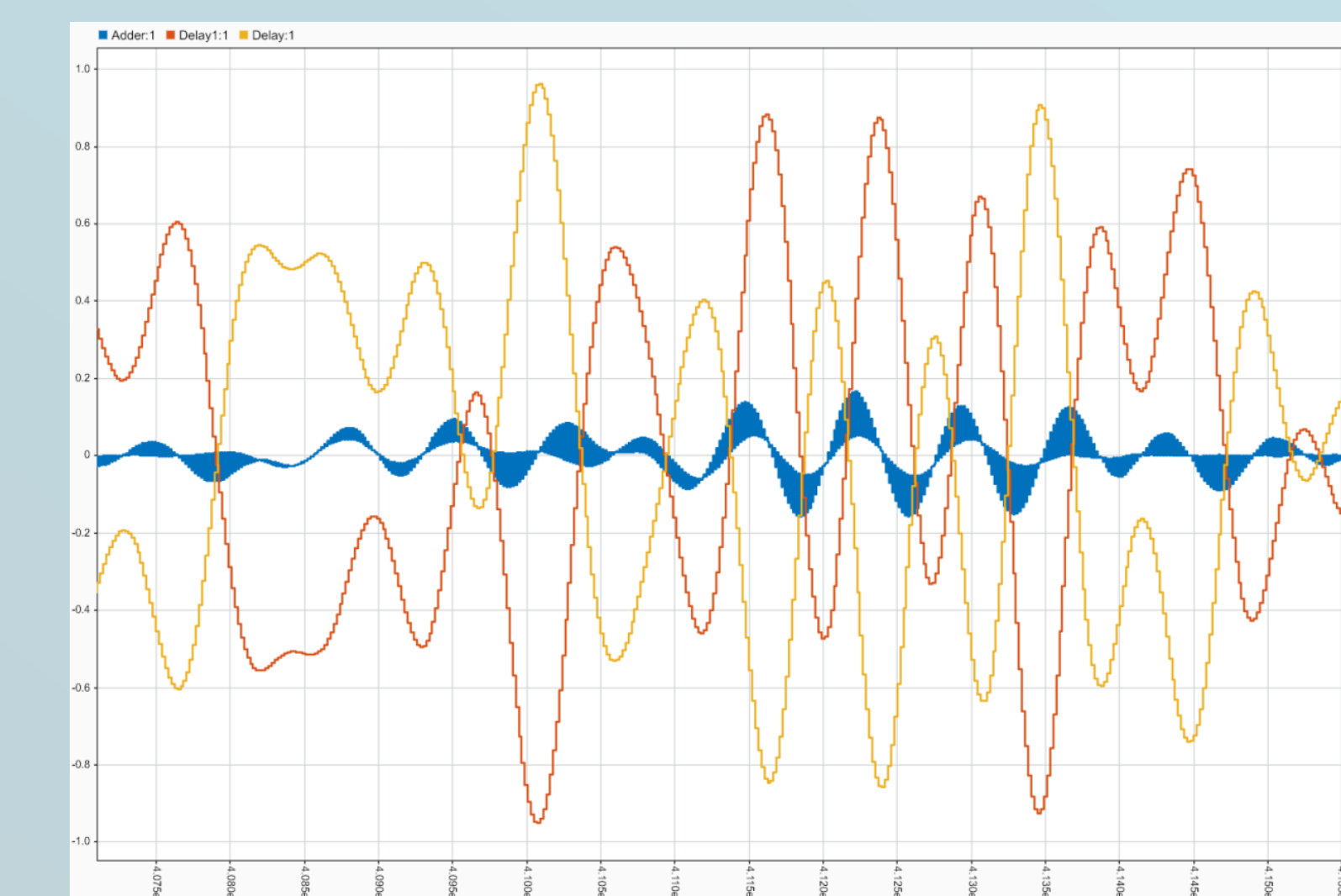


Figure: time-domain noise (orange), anti-noise (yellow) and residual (blue)



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Robert Mehrabian
College of Engineering