RAWR (Radar ASIC Waveform Reciever)

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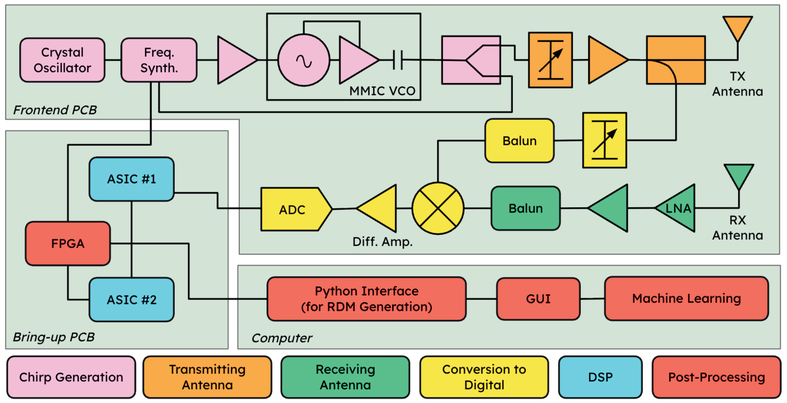
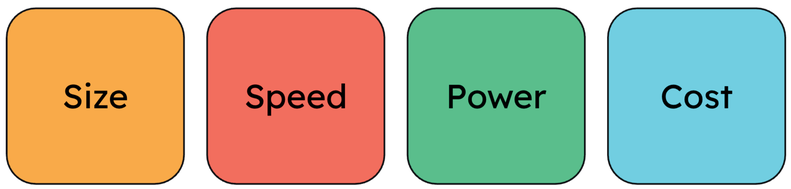
Background

FMCW radar is a reliable sensing technology for autonomous systems because it can measure both object distance and velocity using radio-frequency waves. Unlike cameras and LiDAR, radar remains effective in poor visibility conditions such as fog, rain, snow, and glare, making it valuable for safety-critical platforms including autonomous vehicles, drones, and robotics.

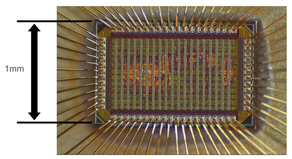


Motivation

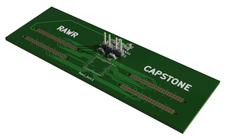


Our core innovation is an Application Specific Integrated Circuit (ASIC) that accelerates the fixed-function stages of a typical RDM-generating radar DSP flow. This pipeline uses a two-ASIC design: the first ASIC performs windowing and the first 1D FFT to generate range data, while the second ASIC performs windowing and the second 1D FFT across chirps to extract Doppler/velocity information. Our design was constrained by the four key metrics shown above.

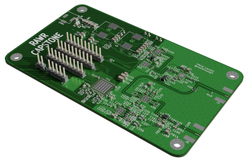
Key Subsystems



ASIC

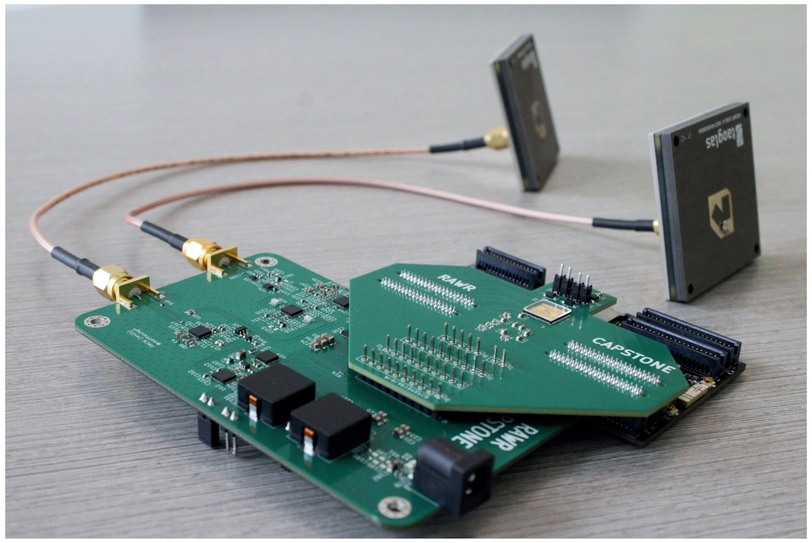


Bring Up Board



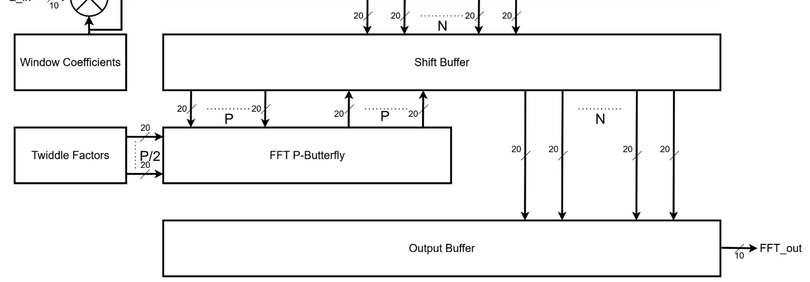
Frontend Board

Final Product



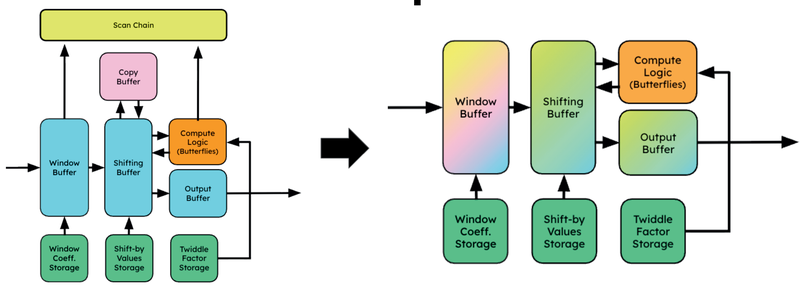
Our fully assembled system for demoing our ASIC shown above contains: antennas, an analog frontend board, a RAWR ASIC setup with two chips, and an FPGA for control and system management.

ASIC Verilog Design

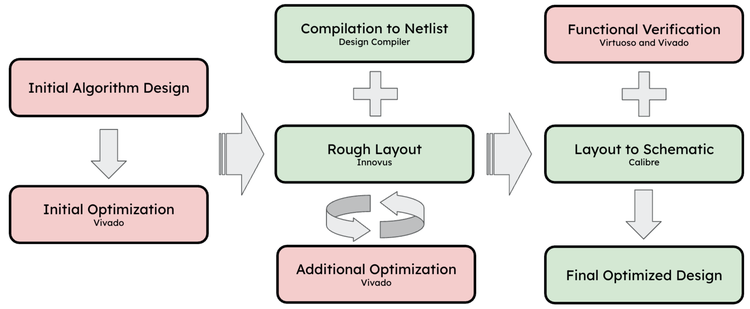


Above is our ASIC diagram showing the flow of data from the input I and Q channels through windowing and a 1D Fast Fourier Transform .

ASIC Area Optimization

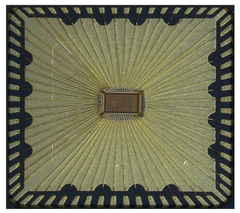


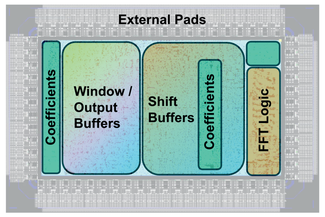
ASIC Design Process



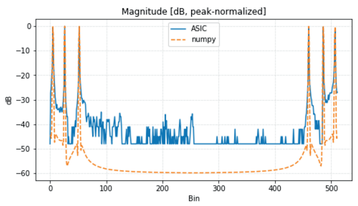
Iterative design process for the RAWR ASIC. Starting with an initial Verilog implementation and progressing through repeated layout optimization until the system met area, power, and timing specifications. Each iteration included verification steps to ensure the final ASIC preserved the intended functionality.

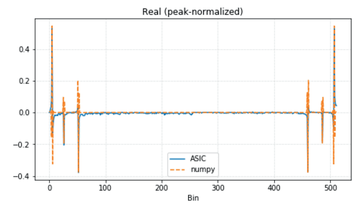
ASIC Packaging and Layout





ASIC Operation Results

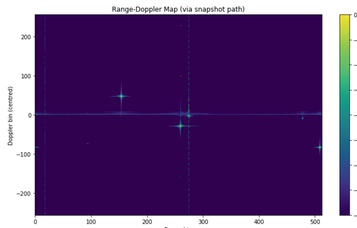




Comparison between the RAWR ASIC output and the NumPy golden model for radar data containing three sinusoidal targets.

	ASIC	FPGA
Cost	$1-3 in Bulk	$100-$300
Area	81mm^2	225-529mm^2
Speed	65 RDM/s	3-15 RDM/s
Power	112mW	400-500mW

Target metric comparison between the RAWR ASIC and equivelent FPGA implementation



Range Doppler Map snapshot taken during operation

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